Claims

1. In a semiconductor manufacturing environment where logic functions are implemented by the coupling together of a plurality of different types of standard cells, each type of standard cell implementing a particular logic function, a method for improving the yield of the integrated circuit through the manufacturing process, the method comprising the steps of:

designing a plurality of different variants for the standard cells in the library, each of the different standard cell variants addressing a different manufacturing problem;

selecting one standard cell variant to be used in a particular manufacturing environment to optimize the resulting yield of integrated circuits fabricated using the selected standard cells; and

coupling together the selected standard cells to implement the logic functions.

2. The method of claim 1 wherein the variants are designed to at least address the manufacturing problems of poor contact formation, contact alignment, metal line spacing and metal line direction changes.

3. The method of claim 1 wherein the variants are each rated for manufacturability, the step of selecting a standard cell variant being influenced by the assigned manufacturability rating.

4. In an integrated circuit design environment wherein multiple standard components are used to form the integrated circuit design, a method for allowing the integrated circuit designer to optimize the integrated circuit design, the method comprising the steps of:

designing a plurality of variants of the standard components;

rating each design variant on at least one variable; and

selecting the design variant whose rating most closely matches the designer's criteria for use in the integrated circuit design.

5. The method of claim 4 wherein the cells of standard components comprise standard logic cells.

6. The method of claim 4 wherein the cells of standard components comprise input/output cells.

7. The method of claim 4 wherein the cells of standard components comprise memory core cells or entire memory blocks including the core cells.

8. The method of claim 4 wherein the cells of standard components perform at least a first analog function, the analog function including one of at least phase locked loops and analog-to-digital converters.

9. The method of claim 4 wherein each of the components and its variants are characterized to indicate the manufacturing yield of the particular variant.

10. The method of claim 4 wherein each variant addresses at least one manufacturing problem.

11. The method of claim 10 wherein the variants of standard components comprise variants of standard logic cells.

12. The method of claim 11 wherein the variants of standard logic cells have each been assigned a rating which indicates its manufacturability in at least a first manufacturing environment.

13. The method of claim 12 wherein the variants of standard logic cells have a plurality of different manufacturability ratings, a different rating being assigned for each different potential manufacturing environment.

14. A system for improving the manufacturability of integrated circuits, the system comprising:

a library comprised of a plurality of variant designs for standard components of the integrated circuit, each of the variant designs compensating for at least a known manufacturing problem;

a design synthesis tool coupled to the library, the synthesis tool formulating and presenting to a user a proposed IC designs, the design incorporating a variant design that corrects for a known manufacturing problem encountered in the particular manufacturing environment selected by the user.

15. The system of claim 14 wherein the library is further comprised of a plurality of variant designs of standard logic cells.

16. The system of claim 15 wherein the variant designs of standard logic cells are rated on a manufacturability index, a different rating being assigned to each variant for each manufacturing environment in which it may be used.

17. The system of claim 14 wherein the library is further comprised of a plurality of variant designs of memory core cells.

18. The system of claim 14 wherein the library is further comprised of a plurality of variant designs of input/output cells.

19. The system of claim 14 wherein the variant designs also include compensation for a design related IC yield limiter, the yield limiters including at least leakage current through transistors.